IN THE SPECIFICATION:

Please amend paragraph **[0002]** as follows:

[0002] State of the Art: Semiconductor devices, from microprocessors to memory chips, are fabricated by performing a long series of processes and steps including etching, masking, ~~depositing and the like~~ depositing, and the like, on a semiconductor wafer or other bulk semiconductor substrate. Many integrated circuits may be fabricated on a single semiconductor wafer by placing them in arrays across the wafer. Ultimately, the individual circuits are singulated from the wafer and are either further processed, including packaging and additional testing, or discarded when they are determined to be undesirable.

Please amend paragraph **[0005]** as follows:

[0005] Conventionally following initial testing, the integrated circuits are singulated into individual integrated circuit chips with the operational chips being further assembled into packages. The packaged devices are then "burned-in" by loading the packaged devices into sockets on burn-in boards and electrically operating the packaged devices at elevated temperatures for an extended testing period. Such elevated temperatures induce failure in marginally operative or nonoperative devices, which allows such devices to be screened-out and discarded before they are integrated into higher level assemblies or sold. Burning-in and testing of packaged devices are typically accomplished through the use of sockets suited for the burn-in conditions and high speed testing. Accordingly, conventional manufacturing and testing processes are expensive and time consuming because of the repeated handling and testing of individual ~~devices,~~ devices; therefore, individually tested and handled devices that ultimately fail have wasted costly resources and time.

Please amend paragraph **[0006]** as follows:

[0006] A considerable advantage in cost and in process time could be attained by burning-in and testing a semiconductor wafer before it is singulated into discrete devices. Additional savings may be recognized by forgoing packaging of devices that ultimately fail once subjected to burn-in conditions. A considerable effort has been expended to develop effective

methods for wafer level testing. One such approach utilizes cantilevered or spring-wire probes ~~which~~ that are arranged on a contact or probe card for simultaneous contact to all of the devices on the semiconductor wafer. Such contactor cards are expensive to manufacture and result in undesirable electrical characteristics such as increased inductance along parallel wires.

Please amend paragraph **[0007]** as follows:

[0007] Therefore, there is a need for providing a contact methodology ~~which~~ that results in a highly economically manufacturable method of contacting individual semiconductor devices in a wafer-level testing environment.

Please amend paragraph **[0008]** as follows:

[0008] Furthermore, individual dice generally need to be packaged into a higher assembly before they may be integrated into a system environment. These higher assemblies or packages generally need to accommodate or compensate for differences in thermal expansion between the individual die and the system level substrate. Therefore, there is a need for providing a contact methodology ~~which~~ that mediates stresses between dissimilar materials.

Please amend paragraph **[0009]** as follows:

[0009] A compliant contact pin assembly, ~~card~~ card, and methods associated ~~therewith~~ therewith, are provided in various embodiments. In one embodiment of the present invention, a contact pin assembly includes a contact pin formed in place from a portion of a substrate. The contact pin is compliantly held suspended within the substrate by a compliant coupling structure. The suspension within the substrate results in a compliant deflection orthogonal to the plane of the substrate.

Please amend paragraph **[0010]** as follows:

[0010] In another embodiment of the present invention, a method for forming a contact pin assembly is provided. A location for the contact pin is defined on a substrate in a location ~~which~~ that corresponds to a target contact pad ~~on a~~, on, for example, ~~wafer~~ a wafer to be tested.

The substrate around the location is thinned for approximately the length of travel of the contact pin on the side defined as the contact end side. The substrate is locally thinned to a depth of at least the length of the contact pin immediately around the location of the contact pin to form a void surrounding the contact pin. The void is filled with compliant coupling material and the opposite side of the substrate is thinned to release the contact pin from the remaining substrate.

Please amend paragraph **[0011]** as follows:

[0011] In another embodiment of the present invention, a method for forming a contact pin assembly wherein the substrate provides the compliant action for the contact pin is provided. The location for the contact pin is defined on the substrate and the substrate is thinned around the location. Further thinning around the contact pin forms a void. The opposite side of the substrate is ~~thinned~~ thinned, but not all the way through to the void. Instead, the remaining substrate on the opposite side flexes when the contact end of the contact pin encounters and presses against a pad on a wafer or other ~~device under test.~~ device-under-test.

Please amend paragraph **[0026]** as follows:

[0026] FIGS. ~~11A-C~~ 11A-11C show a sequence of cross-sectional views illustrating a compliant contact pin assembly, in accordance with another embodiment of the present invention;

Please amend paragraph **[0031]** as follows:

[0031] FIGS. 16A-16F show a sequence of cross-sectional views illustrating a portion of the process steps of a method for fabricating a ~~double sided~~ double-sided compliant contact pin assembly, in accordance with a yet further embodiment of the present invention;

Please amend paragraph **[0032]** as follows:

[0032] FIG. 17 shows a cross-sectional view of a ~~double sided~~ double-sided compliant contact pin assembly, in accordance with a yet further embodiment of the present invention;

Please amend paragraph **[0037]** as follows:

[0037] In FIG. 1A, substrate 10 has defined thereon a location 12 for the formation of a contact pin. Substrate 10 may comprise a silicon wafer, a ceramic substrate, a glass substrate, a quartz substrate, or other suitable material. At the location 12, a mask layer 14 is placed on the top or contact end side of substrate 10. The profile of mask layer 14 identifies the general cross-sectional geometry of an emerging contact pin to be formed at location 12. Mask layer 14 may be thermally grown silicon oxide, CVD silicon ~~oxide~~ oxide, or CVD silicon nitride. Substrate 10 preferably includes a crystal orientation allowing for selectively etching as an isotropic etch. In FIG. 1B, the silicon etch is stopped at a distance 16 corresponding to an approximate contact pin travel distance. The contact travel distance may be heuristically derived as a function of the elasticity or flexibility of the compliant coupling means described below. As illustrated, the etch is preferably an isotropic etch resulting in side walls 18 ~~which~~ that exhibit an approximate orthogonal relationship to thinned contact end surface 20.

Please amend paragraph **[0038]** as follows:

[0038] In FIG. 1C, additional mask layers 22 of the same general nature as mask layer 14 are placed on thinned contact end surface 20 for the formation of stops ~~which~~ that regulate the travel distance of the contact pin under fabrication. It is noted that the stops may be discrete or generally continuous in circumscribing the emerging contact pin formed at location 12.

Please amend paragraph **[0039]** as follows:

[0039] In FIG. 1D, substrate 10 has been further thinned or etched to form stops 24 ~~which~~ that limit the distance of travel of the contact pin as well as provide a stand-off for particles or contaminants that may be present on the further thinned contact end surface 26 of substrate 10. In FIG. 1E, the maximum depth of the emerging contact pin 34 is defined through the formation of a void 28 surrounding the emerging contact pin 34. Void 28 may be formed in one of several manners including a photo etch process, wherein other portions of the substrate are masked and protected from the etching process. Alternatively, void 28 may be formed through

laser ablation or machining. Laser machining may be performed by a micro machining laser such as the XCISE 200 available from XSIL Ltd. of Dublin, Ireland.

Please amend paragraph **[0040]** as follows:

[0040] As illustrated in FIG. 1E, a thickness 30 of substrate 10 remains intact to support the emerging contact ~~pin~~ pin 34 through further manufacturing processes. If substrate 10 is comprised of a semiconductive or conductive material, an insulative layer 31, such as an oxide layer, is formed on the sidewalls of void 28. When substrate 10 is comprised of a nonconductive material, then an insulative layer is unnecessary. In one embodiment, the emerging contact pin 34, in addition to the surfaces defining void 28, are conductively coated by depositing a conductive material 32 generally over the emerging contact pin 34 and throughout the void 28. In one particular embodiment, as illustrated in FIG. 1F, conductive material 32 is formed through a metallic plating ~~process~~ process, which results in conductive surfaces on remaining substrate portions 36 and on emerging contact pin 34.

Please amend paragraph **[0042]** as follows:

[0042] To enable compliant movement relative to the remaining substrate portions 36, the contact pin is released from the remaining substrate portions 36. In FIG. 1H, the back or opposite surface 40 of substrate 10 is thinned, either through an etching process or through a mechanical grinding ~~process~~ process, for at least a thickness or distance 30 to release or free contact pin 42 from adjacent portions of substrate 10. As illustrated, contact pin 42 is formed from a portion of substrate 10 and remains positioned at original location 12 through compliant coupling means, namely compliant coupling material 38.

Please amend paragraph **[0043]** as follows:

[0043] In a specific embodiment as illustrated in FIG. 1I, contact pin 42 is further coated with additional conductive material 44 at a bottom or interconnect ~~end~~ end 51 to encapsulate the contact pin with additional conductive material. Consistent with the formation of conductive material 32 about the contact end 29 of contact pin 42 and throughout void 28,

conductive material 44 may be formed through various processing steps including electroplating or other plating or coating techniques.

Please amend paragraph **[0044]** as follows:

[0044] FIG. 2 illustrates a contact pin assembly 46, in accordance with one embodiment of the present invention. A compliant axis 48 illustrates the axis of motion of contact pin 42 as a result of the resilient or elastic nature of compliant coupling material 38′. Furthermore, in one exemplary embodiment, the compliant coupling material is electrically conductive and is illustrated as compliant coupling material 38′. Electrical continuity exists from contact tip or contact end 50 of contact pin 42 to substrate 10 by way of conductive material 32 electrically coupled with electrically conductive compliant coupling ~~material 38′~~ material 38′, which further is electrically coupled to a portion 52 of the conductive material affixed to the remaining substrate 10. Routing of a signal detected at contact end 50 of contact pin 42 may be further routed via one or more conductive traces 54 to other desirable locations. Conductive trace 54 may be formed according to various interconnection techniques including masking, ~~deposition~~ deposition, and etching techniques, the specifics of which are appreciated by those of ordinary skill in the art.

Please amend paragraph **[0047]** as follows:

[0047] FIG. 5 illustrates a coupling of a device-under-test 56 having a contact pad 58 mating with contact pin assembly 46′. As illustrated, contact pin 42 compliantly deflects along compliant axis 48 due to the resiliency of compliant coupling material 38″. Also illustrated, wire bond 60 further deforms in response to the compliant motion of contact ~~pin 42~~ pin 42, thereby maintaining electrical continuity between contact pin 42 and conductive trace 54.

Please amend paragraph **[0048]** as follows:

[0048] FIGS. 6A-6D illustrate yet another method of formation of a contact pin for use in a contact pin assembly, in accordance with another embodiment of the present invention. In the present embodiment, processing of substrate 10 follows preliminary processing steps

according to FIGS. 1A-1E. Prior thereto, however, a bore 62 is formed entirely through substrate 10, for example, centered within location 12, and through the emerging contact pin. Boring techniques may include those utilized for the formation of voids 28, namely etching and or laser ablating techniques. In FIG. 6B, bore 62 (FIG. 6A) is filled with a conductive ~~material 64~~ material 64, which may be formed using plating, sputtering, squeegeeing or other conductive fill techniques known by those of ordinary skill in the art. This may also be effected prior to the steps of FIGS. 1A-1E. In FIG. 6C, voids 28 (FIG. 6A) are filled with compliant coupling material 38 according to techniques described above with reference to FIG. 1G. In FIG. 6D, an etching or abrasive process, such as mechanical grinding or abrasive planarization such as Chemical Mechanical Planarization (CMP), removes the ~~backside~~ back side of substrate 10 for at least a distance or thickness 30 to release the emerging contact pin to form contact pin 66.

Please amend paragraph **[0049]** as follows:

[0049] FIG. 6E illustrates an alternative approach for releasing the emerging contact pin to form contact pin 67. In the present embodiment of the present invention, contact pin 67 is released by isolating contact pin 67 from remaining substrate portions 69 of substrate 10 by forming voids 71 through one or more substrate removal processes previously described. Such processes include etching, laser ~~machining~~ machining, and mechanical routing, etc.

Please amend paragraph **[0050]** as follows:

[0050] The ends of contact pin 66 are preferably conductively coated to further facilitate electrical coupling. FIG. 7 and FIG. 8 illustrate various contact ends or tips that may be formed upon contact pins 66, 67, in accordance with respective embodiments of the present invention. In FIG. 7, a conductive material 68 is formed to provide electrical continuity with conductive material 64. Conductive material 68 may be formed using plating or other deposition ~~processes~~ processes, which results in a conductive contact surface for mating with device-under-test 56 (FIGS. 3 and 5). In FIG. 8, a bump of conductive material 70 is formed on contact pin 66 for providing electrical continuity with conductive material 64. In the present

embodiment, conductive material 70 may be formed using solder bumping ~~technology~~ technology, such as that utilized in the formation of balls of a ball grid array (BGA) or by using a wire bond capillary to place a bump of conductive material 70. The formation of such conductive bumps is known by those of ordinary skill in the art and is not further described herein.

Please amend paragraph **[0052]** as follows:

[0052] FIG. 9 illustrates a device assembly utilizing a contact pin assembly, in accordance with another embodiment of the present invention. While compliant coupling of a contact pin assembly for temporary interconnection with a device-under-test are illustrated herein, various embodiments of the present invention also find application when permanently coupled with one or more devices to form a device assembly for further integration or coupling with a substrate, such as a printed circuit board. A device assembly 112 includes a contact pin assembly 102, formed in accordance with the one or more embodiments described herein, and one or more devices 104 permanently coupled thereto. The one or more devices 104 include one or more contact pads 108 ~~which~~ that electrically interface with the one or more contact pins 106 of the contact pin assembly 102. The device assembly 112 may then be further coupled to outer lead contact pads 110 on a substrate 114. Electrical coupling techniques for coupling devices 104 to substrate 114 via the contact pin assembly 102 are appreciated by those of ordinary skill in the art and therefore are not further described herein.

Please amend paragraph **[0054]** as follows:

[0054] FIG. 10 illustrates a device assembly utilizing a contact pin assembly, in accordance with yet another embodiment of the present invention. In the present embodiment, a redistribution layer may be implanted through the use of a contact pin assembly external to the active devices. Those of skill in the art appreciate that additional processing steps performed on active devices results in a decreased yield of operation devices due to the additional handling and processing parameters, such as elevated temperatures. Therefore, in the present embodiment, the redistribution of inner lead contact pads 118 to outer lead ~~bond~~ contact pads 110 is accomplished

through coupling a contact pin assembly 122 to a device 104. Specifically, a device assembly 132 includes a contact pin assembly 122, formed in accordance with the one or more embodiments described herein, and one or more devices 104 permanently coupled thereto. The one or more devices 104 include one or more inner lead contact pads 118 ~~which~~ that electrically interface with the one or more contact pins 116 of the contact pin assembly 122. The device assembly 132 may then be further coupled to outer lead contact pads 110 on a substrate 114. Electrical coupling techniques for coupling devices 104 to substrate 114 via the contact pin assembly 102 are appreciated by those of ordinary skill in the art and therefore are not further described herein.

Please amend paragraph **[0055]** as follows:

[0055] Coupling of a device 104 to a substrate 114 via a contact pin assembly 122 finds application by providing an intermediary expansion medium, namely the contact pin assembly 122, for mediating variations in the expansion and redistributing interconnects from an inner lead contact pad 118 to an outer lead contact pad 110. Electrical continuity between contact pads 108 and 110 ~~are~~ is maintained by the compliant coupling material of the contact pins 116 and a redistribution conductive trace 124 within the contact pin assembly 122.

Please amend paragraph **[0056]** as follows:

[0056] FIGS. 11A-11C illustrate yet another embodiment of a contact pin for use in a contact pin assembly, in accordance with embodiments of the present invention. In the present embodiment, additional compliance is provided by the extension of a conductive material beyond the thinned ~~backside~~ back side surface of substrate 10 or, in yet another embodiment, through the capping of the contact pin with compliant conductive "bricks" or "blocks." In the present embodiments, processing of substrate 10 undergoes processes described above for the formation of a void 28 surrounding the emerging contact pin 234. Void 28 may be formed in one of several manners described above including a photo etch process, laser ~~machining~~ machining, or mechanical drilling.

Please amend paragraph **[0057]** as follows:

[0057] A bore 262 is formed entirely through substrate 10, exemplary centered about location 12, and through the emerging contact ~~pin~~ pin 234. Boring techniques may include those utilized for the formation of voids 28, namely etching ~~and or~~ and/or laser ablating techniques. In FIG. 11B, bore 262 (FIG. 11A) is filled with a conductive ~~material 264~~ material 264, which may be formed from a conductive polymer. While the filling process may be done using various techniques, two exemplary techniques, include squeegeeing the material through, or drawing the material through bore 262, are contemplated. In FIG. 11C, voids 28 are filled with compliant coupling material 38 according to techniques described above with reference to FIG. 1G and the contact pin is released from the remaining substrate portions, according to the process described above with reference to FIG. 1H, wherein the back or opposite surface of substrate 10 is thinned, either through an etching process or through a mechanical grinding process.

Please amend paragraph **[0058]** as follows:

[0058] FIGS. 12A-C and 13A-C illustrate separate embodiments for releasing the emerging contact pin 234 (FIG. 11A) from the remaining substrate portions and for electrically capping the contact pin. In FIG. 12A, a masking and etching process is used to remove the ~~backside~~ back side of substrate 10 from surface 240 for at least a distance 230 to release the emerging contact pin to form contact pin 266. FIG. 13A illustrates an alternative approach for releasing the emerging contact pin to form contact pin 267. In the embodiment as illustrated in FIG. 13A, contact pin 267 is released by isolating contact pin 267 from remaining substrate portions 269 of substrate 10 by forming voids 71 through one or more substrate removal processes previously described. Such processes include masking and etching, laser machining and mechanical routing, etc.

Please amend paragraph **[0059]** as follows:

[0059] The ends of contact pins 266, 267 are preferably coated to further facilitate electrical coupling and/or to extend the end of the contact pin above the substrate. FIG. 12B and FIG. 13B illustrate various contact ends or tips that may be formed upon contact pins 266, 267,

in accordance with respective embodiments of the present invention. In FIG. 12B, conductive material 268 and 272 are formed to provide electrical continuity with conductive material 264. Conductive material 268 and 272 may be formed using plating or other deposition processes, including the formation of conductive polymer bricks or ~~blocks~~ blocks, which results in a conductive contact surface for mating with contact pad 58 of device-under-test 56 (FIG. 12C). In FIG. 13B, ~~a conductive~~ conductive material 270 is formed on contact pin 267 for providing electrical continuity with conductive material 264. In the present embodiments, conductive material 270 and 274 may be formed using, for example, conductive deposition techniques described above, conductive polymer bricks on the top and/or bottom of contact ~~pin 267~~ pin 267, which results in a conductive contact surface for mating with contact pad 58 of a device-under-test 56 (FIG. 13C). Conductive material 270 and 274 formed of conductive polymers may provide additional compliant force due to the intrinsic compressibility of, for example, the polymer.

Please amend paragraph **[0060]** as follows:

[0060] As a further enhancement to the contact pin 267, while the conductive material 270, 274, is in a "wet" or semi-cured state, flakes of material such as dendritic material for scrubbing the material to be probed by the contact pin may be applied to conductive material 270, 274. FIGS. 12C and 13C further illustrate the formation of one or more conductive traces 254, 255 and the electrical coupling of conductive material 264 with a yet further conductive material 268, 272 and ~~270, 274~~ 270, 274, for providing electrical conduction with a conductive compliant material 238.

Please amend paragraph **[0064]** as follows:

[0064] In FIG. 14B, the silicon etch is stopped at a distance 120 corresponding to an approximate contact pin travel distance. The contact travel distance may be heuristically derived as a function of the elasticity or flexibility of the compliant coupling means described, and, for one application, may be on the order of 75 μm. As illustrated, the etch is preferably an isotropic

etch resulting in the side ~~walls 422~~ walls 422, which exhibit an approximate pyramidal relationship to thinned contact end surface 424.

Please amend paragraph **[0065]** as follows:

[0065] In FIG. 14C, the depth of the emerging contact pin is generally defined through the formation of a void 126 surrounding the emerging contact pin. Void 126 may be formed in one of several manners including a photo etch process wherein other portions of the substrate are masked and protected from the etching process. Alternatively, void 126 may be formed through laser ablation or machining, as described above with reference to ~~FIG. 1.~~ FIG. 1E. As illustrated in FIG. 14C, a thickness 128 of substrate 10 remains intact to support the emerging contact pin through further manufacturing processes. When substrate 10 is semiconductive or conductive, an insulating oxide layer 127 is formed within void 126 to insulate any electrical signals from becoming shorted or exhibiting ~~crosstalk.~~ cross-talk.

Please amend paragraph **[0066]** as follows:

[0066] In FIG. 14D, the emerging contact pin 432 in addition to the surfaces of void 126 are conductively coated by depositing a conductive material 130 generally over the emerging contact pin 432 and throughout the void 126. Conductive material 130 may be formed through a metallic plating process, sputtering process, or other particle deposition ~~process~~ process, which results in conductive surfaces on remaining substrate portions 134 and on emerging contact pin 432.

Please amend paragraph **[0067]** as follows:

[0067] A compliant coupling structure couples emerging contact pin 432 with remaining substrate portions 134 of substrate 10. By way of example and not limitation, FIG. 14E illustrates one such structure as compliant coupling material 136. Compliant coupling material 136 at least partially fills void 126 and forms a flexible or compliant interface between emerging contact pin 432 and remaining substrate portions 134 of substrate 10. In FIG. 14F, the back or opposite surface 138 of substrate 10 is thinned either through an etching process or

through a mechanical grinding or abrasion process for at least a thickness or distance 140 to release or free contact pin 142 from adjacent substrate portions 134 of substrate 10. As illustrated, contact pin 142 is formed from a portion of substrate 10 and remains positioned at original location ~~412~~ through compliant coupling means, namely compliant coupling material 136.

Please amend paragraph **[0068]** as follows:

[0068] In FIG. 14G, contact pin assembly 144 may further include a redistribution layer, such as conductive trace 146, for electrically routing contact pin 142 to a separate location. FIG. 14G further illustrates a via 148 ~~which~~ that may further electrically couple conductive trace 146 to an opposite side 150 of substrate portions 134 of substrate 10 for further routing on opposite side 150 or for coupling with a probe 152 at a contact pad 154. Additionally, contact pin 142 may be further coated with additional conductive material 156 at a bottom or interconnect end to encapsulate the contact pin 142. Consistent with the formation of conductive material 130 (FIG. 14D) about the ~~contact~~ contact end of contact pin 432 and throughout void 126, conductive material 156 may be formed through various processing steps including plating, ~~sputtering~~ sputtering, or other coating approaches.

Please amend paragraph **[0069]** as follows:

[0069] FIG. 15 shows a cross-sectional view illustrating a compliant contact pin assembly, according to yet another embodiment of the present invention. The present embodiment accommodates inline probing of the back of the contact ~~pin 162~~ pin 162, without subjecting the contact pad of a device-under-test to the damaging effects of a direct probe. A contact pin assembly 158 is generally fabricated according to the steps of FIGS. 14A-14E, however, a via 160 is formed, for example through laser machining, through the contact pin 162. Via 160 is then filled with a conductive material 164 for electrically coupling the contact end 163 of contact pin 162 with the opposite side 170 of contact pin assembly 158. An additional contact pad 166 may be further formed for direct probing by a probe 168.

Please amend paragraph **[0070]** as follows:

[0070] FIGS. 16A-16F and FIG. 17 show cross-sectional views illustrating various embodiments of ~~dual sided~~ dual-sided compliant contact pin assemblies. These embodiments facilitate the formation of compliant contacts on both sides of a contact pin assembly to accommodate an offset configuration or a redistribution arrangement.

Please amend paragraph **[0071]** as follows:

[0071] In FIG. 16A, substrate 10 has defined thereon a region or location 312 for the formation of a ~~dual sided~~ dual-sided contact pin assembly. In the present embodiment, the contact pin assembly is comprised of a contact pin on each surface or side of the substrate 10 that are electrically coupled together. At the location 312, an emerging contact pin 334 on a first side 314 is located and defined through the formation of voids 328, according to one or more of the substrate removal techniques ~~describe~~ described above, surrounding the emerging contact pin 334. A via void 316 is also formed partially through substrate 10 also using one or more of the substrate removal techniques ~~describe~~ described herein. Via void 316 provides an aperture for the formation of an electrical connection therethrough between first side 314 and second side 315.

Please amend paragraph **[0072]** as follows:

[0072] In FIG. 16B, an emerging contact pin 335 is defined through the formation of voids 329 surrounding emerging contact pin 335, according to one or more of the substrate removal techniques described herein. A via void 317 provides an aperture partially through substrate 10 from second side 315. Via voids 316 and 317 form a via void through the entire thickness of substrate 10 accommodating the formation of electrical continuity between the contact ~~pins~~ pins 334, 335 formed on sides 314 and 315.

Please amend paragraph **[0073]** as follows:

[0073] When laser machining or other coarse substrate removal techniques are used, a cleaning process may further be utilized to soften any rough edges and to clean any scorched

substrate from the respective voids. By way of example and not limitation, exemplary cleaning processes may include TetraMethyl Ammonium Hydroxide (TMAH) or Propylene Glycol TMAH as the etching agent. Such substrate post-process cleaning processes are contemplated and the specific application of these processes is known by those of ordinary skill in the art ~~and are~~ and is not further described herein.

Please amend paragraph **[0074]** as follows:

[0074] As illustrated in FIG. 16C, if substrate 10 is comprised of a semiconductive or conductive material, an insulative layer 331, such as an oxide layer, is formed on the sidewalls of voids 328, 329 and via voids 316, 317. When substrate 10 is comprised of a nonconductive material, then an insulative layer is unnecessary. In one embodiment, the emerging contact pins 334 and 335 in addition to the surfaces of voids 328, 329 and via voids 316, 317 are conductively coated by depositing a conductive material 32 generally over the emerging contact pins 334 and 335 and throughout the voids 328, 329. Conductive material 32 is further deposited about via voids 316, 317 forming a conductive via 319. In one particular embodiment, conductive material 32 is formed through a metallic plating process ~~which~~ that results in conductive surfaces.

Please amend paragraph **[0075]** as follows:

[0075] As illustrated in FIG. 16D, a compliant coupling structure couples emerging contact pins 334 and 335 with surrounding remaining portions 336 of substrate 10. By way of example and not limitation, one such structure is compliant coupling material 38. Compliant coupling material 38 at least partially fills voids 328 and 329 and forms a resilient compliant interface between emerging contact pins 334 and 335 with remaining substrate portions 336 of substrate 10. Suitable compliant coupling materials were described above with reference to ~~FIG. 1.~~ FIG. 1G. In another embodiment, conductive via 319 may be further filled with compliant coupling material 38 in lieu of voids 328, 329 from being filled.

Please amend paragraph **[0077]** as follows:

[0077] FIG. 16F illustrates a contact pin assembly 346, in accordance with one embodiment of the present invention. Compliant axis 348 relative to contact pin 342 and compliant axis 349 relative to contact pin 343 illustrate the axis of motion of contact pins ~~342, 343~~ 342, 343, as a result of the resilient or elastic nature of compliant coupling material 38. Furthermore, in one exemplary embodiment, the compliant coupling material is electrically conductive and is illustrated as compliant coupling material 38. Electrical continuity exists from contact tip or contact end 350 of contact pin 342 to substrate 10 by way of conductive material 32 electrically coupled with electrically conductive compliant coupling ~~material 38~~ material 38, which further is electrically coupled to a portion 352 of the conductive material affixed to the remaining substrate 10. Routing of an electrical signal detected at contact end 350 of contact pin 342 may be further routed via one or more conductive traces 354 to conductive via 319. Similarly, electrical continuity exists from contact tip or contact end 351 of contact pin 343 to substrate 10 by way of conductive material 32 electrically coupled with electrically conductive compliant coupling ~~material 38~~ material 38, which further is electrically coupled to a portion 353 of the conductive material affixed to the remaining substrate 10. Routing of a signal detected at contact end 351 of contact pin 343 may be further routed via one or more conductive traces 355 to conductive via 319. Conductive traces 354, 355 may be formed according to various interconnection techniques including masking, ~~deposition~~ deposition, and etching techniques, the specifics of which are well known to those of ordinary skill in the art.

Please amend paragraph **[0079]** as follows:

[0079] FIG. 18 illustrates a contact pin assembly 74, in accordance with another embodiment of the present invention. The processing steps for the formation of contact pin assembly 74 occur according to the processing steps of FIGS. 6A-6B to form voids 76 around contact pin 78 with the center bore being filled with a conductive material 80 coupled to an electrical trace 82. According to the present embodiment, a compliant coupling structure provides the compliant action for contact pin 78. In the present embodiment, the compliant

coupling structure, by way of example and not limitation, is implemented as a thinned substrate web 84 ~~which~~ that is thinned according to the corresponding widths of voids 76. The thinning process enables contact pin 78 to flex, as illustrated in FIG. 19, when a device-under-test 56 having a contact pad 58 is coupled therewith. Additionally, according to FIG. 18, various contact ends or tips 86 may be formed according to deposition, ~~plating~~ plating, or other processes known by those of ordinary skill in the art.

Please amend paragraph **[0080]** as follows:

[0080] FIG. 20 illustrates a testing system utilizing one or more embodiments of the contact pin assemblies described above. A device-under-test such as a semiconductor wafer 88 having one or more contact pads 90 thereon is coupled with a contactor ~~card 92~~ card 92, which includes one or more contact pin assemblies 94. The contact pin assemblies 94 are further coupled with a tester 96 to form a test system 98. Contactor card 92 on semiconductor wafer 88 may be physically or mechanically coupled through the application of force, or may be coupled together through the use of air pressure as generated by a vacuum 100.